IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: Unknown
Examiner: Unknown

In re Patent Application of

Applicant	:	Liu Guo LIN
Application No.	:	Unknown (Divsional of 09/663,692)
Filed	:	December 21, 2001
For	:	STRUCTURE OF SEMICONDUCTOR ELECTRONIC DEVICE AND METHOD OF MANUFACTURING THE SAME
Attorney Docket	:	32014-177429

PRELIMINARY AMENDMENT

December 21, 2001

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the application as follows:

IN THE SPECIFICATION:

Please replace the paragraph beginning at page 3, line 8, with the following rewritten paragraph:

Typical embodiments of the present invention have been shown in brief. However, the various embodiments of the present invention and specific configurations of these embodiments will be understood from the following description.

Please replace the paragraph beginning at page 4, line 27, with the following rewritten paragraph:

Figs. 1 and 2 are respectively structure cross-sectional views for describing a first embodiment of the present invention. In a structure suitable for use in a semiconductor electronic device using an SOI substrate, structures convex toward the SOI substrate side are provided below side walls on the sides of a gate electrode after the formation of the gate electrode as designated at symbols a and a' in Fig. 1. The shape of each structure may be arcuate. Alternatively, their shapes may be rectangular as designated at symbols b and b' in Fig. 2.

Please replace the paragraph beginning at page 5, line 19, with the following rewritten paragraph:

In the structures according to the present invention as shown in Figs. 1 and 2, no silicides dive under the side walls. The resultant device can achieve a reduction in gate leakage current, an increase in gate withstand voltage and an improvement in short channel effect.

Please replace the paragraph beginning at page 8, line 4, with the following rewritten paragraph:

When the silicides are formed over the source, drain and gate electrodes through the use of the side wall structure formed by the above-described method, the silicidation at the source and drain is blocked by the oxide film convex downwardly toward the SOI substrate, thus causing no transverse growth of the silicides below the gate oxide film.

Please replace the paragraph beginning at page 8, line 21, with the following rewritten paragraph:

Fig. 5 is a process cross-sectional view for describing a fourth embodiment of the present invention. As shown in Fig. 5(1), a gate electrode is formed and thereafter an oxide film (SiO_2) used for first side walls is deposited thereon by a CVD method or the like. Further, as shown in Fig. 5(2), first side wall etching is effected with dry etching using CF_4 gas or the like, and a trenching effect at each edge is utilized to etch even Si of an SOI layer at the edge. As shown in Fig. 5(3), the exposed Si is further etched by using an Si etching solution such as an ammonia solution of 1-30% or a hydrofluoric acid + hydrogen peroxide solution or the like. Next, as shown in Fig. 5 (4), the exposed Si (etched portions) is oxidized to form oxide films identical in quality to a gate oxide film. Next, side walls are formed again as shown in Fig. 5(5). Consequently, portions below the side walls respectively have shapes convex downwardly toward the SOI layer.

Please replace the paragraph beginning at page 9, line 12, with the following rewritten paragraph:

When the side wall structure formed by the above-described method is utilized to allow Si to react with a metal for the purpose of forming silicides, the silicides are blocked by the oxide films convex downwardly toward the SOI layer and hence no transverse growth of silicides below the gate oxide film occurs. Further, the degree of convexity of the oxide film toward the SOI substrate side can be adjusted by etching before the side walls are formed again by the CVD method or the like. Thus, the present embodiment also has the advantage that the degree of downward convexity of the oxide film can be controlled according to the thickness of each silicide layer.

Please replace the paragraph beginning at page 11, line 20, with the following rewritten paragraph:

In the structure of the present invention as shown in Fig. 6(7), the degree of convexity of the oxide film below each side wall into the SOI substrate can be controlled by varying the thickness of the silicides upon formation, with respect to each other. The silicides do not get under the side walls upon formation when the silicide films differ in thickness from each other. Further, silicide edges can be steeply controlled in the vertical direction along the sides of the side walls. The resultant device can achieve not only an increase in gate withstand voltage but also a decrease in gate leakage current.

Please replace the paragraph beginning at page 14, line 4, with the following rewritten paragraph:

When silicides E'' are formed through the use of the side wall structures formed by the above-described method, silicides as designated at D'' are formed even outside the side walls as shown in Fig. 8(3). However, no silicides are formed below the gate oxide film A''. The lower sides of the side walls C'' are not silicided, because the Poly-Si or amorphous Si D'' is easier to silicide than the Si of an SOI substrate.

IN THE CLAIMS:

Please cancel claims 1-4.

Please amend claim 5 as follows:

5. (Amended) The method as claimed in claim 5, wherein said substrate is an SOI substrate or an Si substrate.

Please add claims 11-14 as follows:

--11. The method as claimed in claim 6, wherein said substrate is an SOI substrate or an Si substrate.

12. The method as claimed in claim 7, wherein said substrate is an SOI substrate or an Si substrate.

13. The method as claimed in claim 8, wherein said substrate is an SOI substrate or an Si substrate.

14. The method as claimed in claim 9, wherein said substrate is an SOI substrate or an Si substrate. --

IN THE DRAWINGS:

A concurrently filed Request for Approval of Drawing Changes requests that Figs. 6-8 be amended as shown in red ink. The drawings were amended for clarification purposes. The approval of the Examiner is requested.

REMARKS

This application is a divisional application. Claims 1-4 have been canceled, claim 10 amended, and claims 11-14 added to the application. Further, the specification, and Figures 6-8 have been editorially amended. The attachment to this Amendment entitled "Version with Markings to Show Changes Made" is a marked-up version of the changes made to the specification and the claims. The pending claims correspond to Group II, as set forth in the Restriction mailed December 4, 2000 in the parent application, U.S. Patent Application No. 09/663,692, filed September 19, 2000. Applicant hereby requests an action on the merits at the earliest opportunity for claims 5-14 corresponding to Group II.

Respectfully submitted,

Michael A. Sartori, Ph.D.
Registration No. 41,289
VENABLE
P.O. Box 34385
Washington, DC 20043-9998
Telephone: (202) 926-4800
Telefax: (202) 962-8300

MAS/ab
DC2-339794

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning at page 3, line 8, is amended as follows:

Typical embodiments [ones of various inventions] of the present invention [application] have been shown in brief. However, the various embodiments [inventions] of the present invention [application] and specific configurations of these embodiments [inventions] will be understood from the following description.

The paragraph beginning at page 4, line 27, is amended as follows:

Figs. 1 and 2 are respectively structure cross-sectional views for describing a first embodiment of the present invention. In a structure suitable for use in a semiconductor electronic device using an SOI substrate, structures convex toward the SOI substrate side are provided below side walls on the sides of a gate electrode after the formation of the gate electrode as designated at symbols a and a' in Fig. 1. The shape of each structure may be arcuate [accurate]. Alternatively, their shapes may be rectangular as designated at symbols b and b' in Fig. 2.

The paragraph beginning at page 5, line 19 is amended as follows:

In the structures according to the present invention as shown in Figs. 1 and 2, no silicides dive[s] under the side walls. The resultant device can achieve a reduction in gate leakage current, an increase in gate withstand voltage and an improvement in short channel effect.

The paragraph beginning at page 8, line 4 is amended as follows:

When the silicides are formed over the source, drain and gate electrode[s] through the use of the side wall structure formed by the above-described method, the silicidation at the source and drain is blocked by the oxide film convex downwardly toward the SOI substrate, thus causing no transverse growth of the silicides below [downward of] the gate oxide film.

The paragraph beginning at page 8, line 21, is amended as follows:

Fig. 5 is a process cross-sectional view for describing a fourth embodiment of the present invention. As shown in Fig. 5(1), a gate electrode is formed and thereafter an oxide film (SiO_2) used for first side walls is deposited thereon by a CVD method or the like. Further, as shown in Fig. 5(2), first side wall etching is effected with dry etching using CF_4 gas or the like, and a trenching effect at each edge is utilized to etch even Si of an SOI layer at the edge. As shown in Fig. 5(3), the exposed Si is further etched by using an Si etching solution such as an ammonia solution of 1-30% or a hydrofluoric acid + hydrogen peroxide solution or the like. Next, as shown in Fig. 5 (4), the exposed Si (etched portions) is [are] oxidized to form oxide films identical in quality to a gate oxide film. Next, side walls are formed again as shown in Fig. 5(5). Consequently, portions below the side walls respectively have shapes convex downwardly toward the SOI layer.

The paragraph beginning at page 9, line 12, is amended as follows:

When the side wall structure formed by the above-described method is utilized to allow Si to react with a metal for the purpose of forming silicides, the silicides are blocked by the oxide films convex downwardly toward the SOI layer and hence no transverse growth of silicides

below [downward of] the gate oxide film occurs. Further, the degree of convexity of the oxide film toward the SOI substrate side can be adjusted by etching before the side walls are formed again by the CVD method or the like. Thus, the present embodiment also has the advantage that the degree of downward convexity of the oxide film can be controlled according to the thickness of each silicide layer.

The paragraph beginning at page 11, line 20, is amended as follows:

In the structure of the present invention as shown in Fig. 6(7), the degree of convexity of the oxide film below each side wall into [downward of] the SOI substrate can be controlled by varying the thickness of the silicides upon formation, with respect to each other [according to the thickness of the silicides upon formation of the silicides different in thickness from each other]. The silicides do not get under the side walls upon formation when the silicide films differ[ent] in thickness from each other. Further, silicide edges can be steeply controlled in the vertical direction along the sides of the side walls. The resultant device can achieve not only an increase in gate withstand voltage but also a decrease in gate leakage current.

The paragraph beginning at page 14, line 4, is amended as follows:

When silicides E'' are formed through the use of the side wall structures formed by the above-described method, silicides as designated at D'' are formed even outside the side walls as shown in Fig. 8 (3). However, no silicides are formed below the gate oxide film A''. [This is why, since the Poly-Si or amorphous Si D'' rather than Si of an SOI substrate is easy to silicide,] The lower sides of the side walls C'' are not silicided[.], because the Poly-Si or amorphous Si D'' is easier to silicide than the Si of an SOI substrate.

IN THE CLAIMS:

5. (Amended) The method as claimed in claim 5 [claims 5 to 9], wherein said substrate is an SOI substrate or an Si substrate.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: Unknkown
Examiner: Unknown

In re Patent Application of:

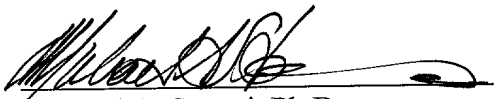
Applicant:	Liu Guo LIN	)
Appln. No.:	Unknown (Divsional of 09/663,692)	) **REQUEST FOR APPROVAL OF DRAWING CHANGES**
Filed:	December 21, 2001	)
For:	STRUCTURE OF SEMICONDUCTOR ELECTRONIC DEVICE AND METHOD OF MANUFACTURING THE SAME	) December 21, 2001
Atty. Docket:	32014-177429	

Assistant Commissioner for Patents
Washington, DC 20231
ATTENTION: OFFICIAL DRAFTSPERSON

Sir:

Pursuant to the provisions in 37 C.F.R. § 1.121(d), Applicant requests approval of the drawing changes shown in red ink for Figures 6-8 on the attached three sheets.

Respectfully submitted,



Michael A. Sartori, Ph.D.
Registration No. 41,289
VENABLE
P.O. Box 34385
Washington, D.C. 20043-9998
Telephone: (202) 926-4800
Telefax: (202) 962-8300

MAS/ab
DC2-339789

Fig.6

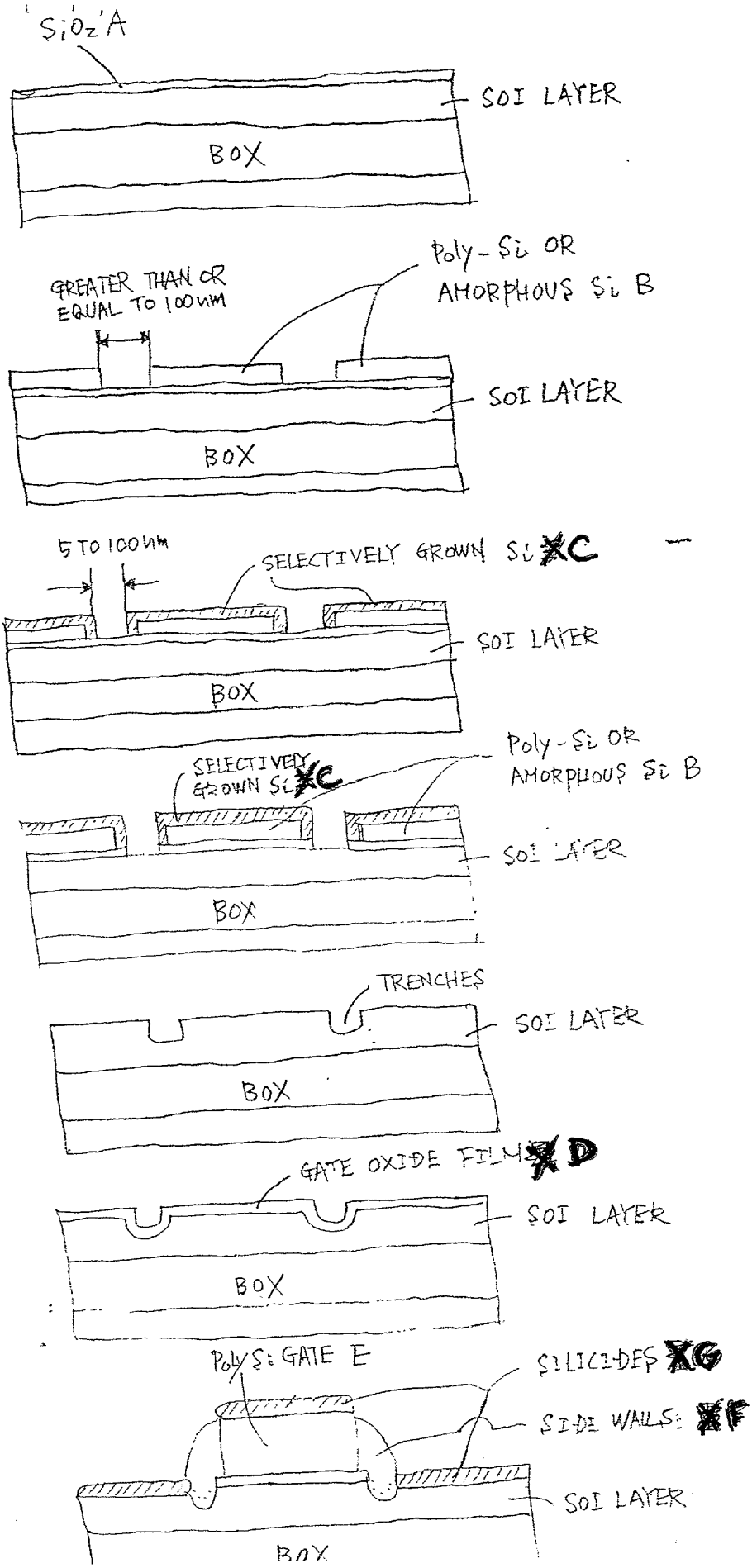
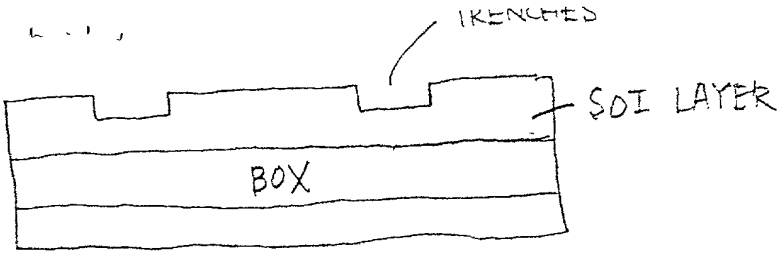
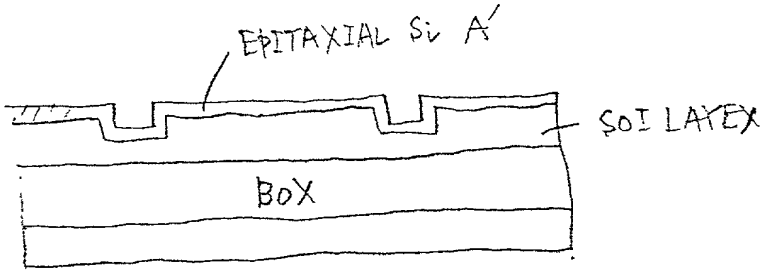

SiO2 'A
SOI LAYER
BOX
(1)
GREATER THAN OR EQUAL TO 100nm
Poly-Si OR AMORPHOUS Si B
SOI LAYER
BOX
(2)
5 TO 100nm
SELECTIVELY GROWN Si XC
SOI LAYER
BOX
(3)
SELECTIVELY GROWN Si XC
Poly-Si OR AMORPHOUS Si B
SOI LAYER
BOX
(4)
TRENCHES
SOI LAYER
BOX
(5)
GATE OXIDE FILM XD
SOI LAYER
BOX
(6)
Poly Si GATE E
SILICIDES XG
SIDE WALLS XF
SOI LAYER
BOX
(7)

Fig. 7

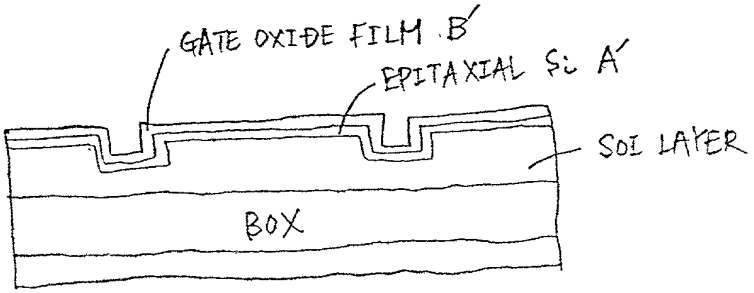
(1)


TRENCHES
SOI LAYER
BOX

(2)


EPITAXIAL Si A'
SOI LAYER
BOX

(3)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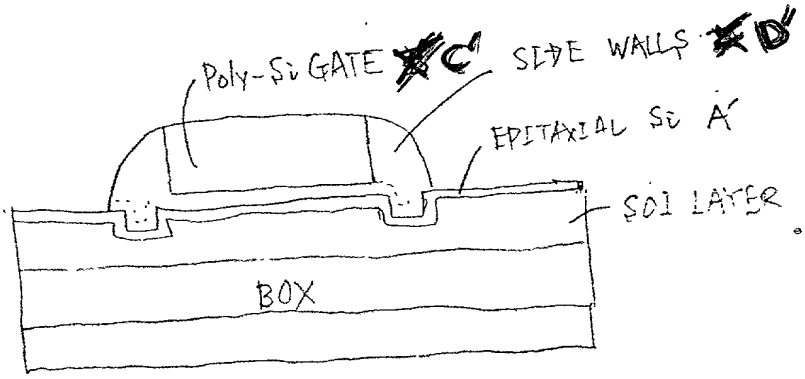
EPITAXIAL Si A'
SOI LAYER
BOX

(4)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SIDE WALLS D'
EPITAXIAL Si A'
SOI LAYER
BOX

(5)

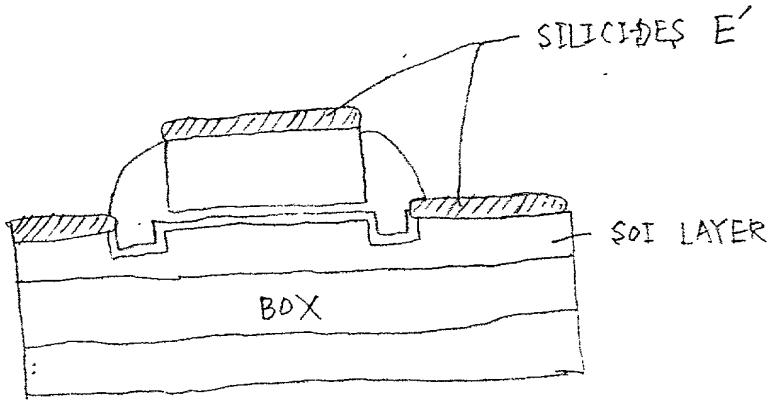
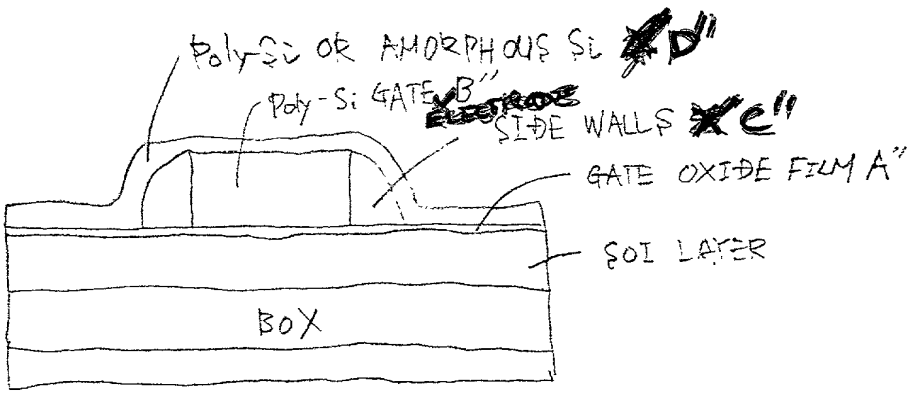
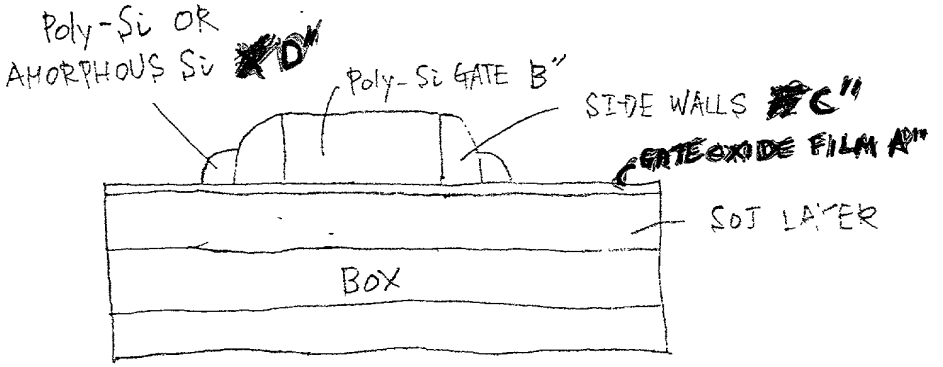

SILICIDES E'
SOI LAYER
BOX

Fig. 8

(1)


Poly-Si OR AMORPHOUS Si "D"
Poly-Si GATE "B"
ELECTRODE
SIDE WALLS "C"
GATE OXIDE FILM A"
SOI LAYER
BOX

(2)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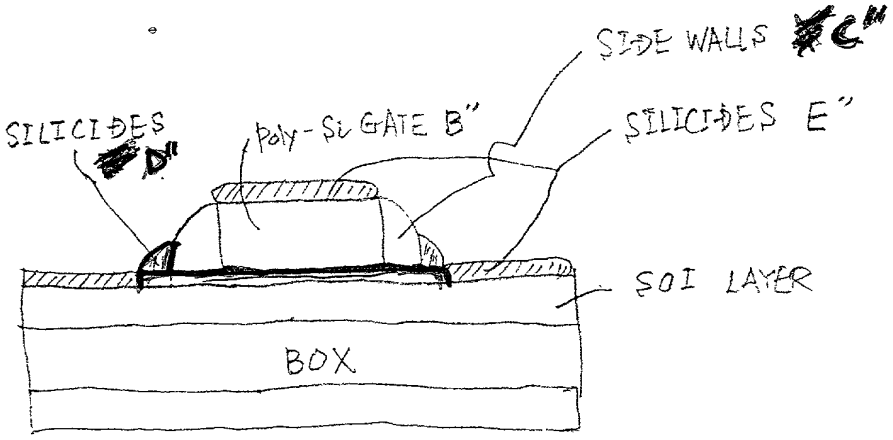
Poly-Si GATE B"
SIDE WALLS "C"
GATE OXIDE FILM A"
SOI LAYER
BOX

(3)


SIDE WALLS "C"
SILICIDES "D"
Poly-Si GATE B"
SILICIDES E"
SOI LAYER
BOX